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# THIN-FILM POLYCRYSTALLINE SILICON SOLAR CELL AND MANUFACTURING METHOD THEREFOR

Patent Number: JP2002261305
Publication date: 2002-09-13
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Requested Patent: ☐ JP2002261305
Application Number: JP20010055130 20010228
Priority Number(s):
IPC Classification: H01L31/04
EC Classification:
Equivalents:

## Abstract

PROBLEM TO BE SOLVED: To provide a thin-film polycrystalline silicon solar cell having superior photoelectric conversion characteristics and to provide a manufacturing method, by which the thin film polycrystalline silicon solar cell is efficiently and easily obtained. SOLUTION: A p-type polycrystalline silicon layer 3 of this thin-film polycrystalline silicon solar battery 10 is composed of a first layer 32 and a second layer 34, successively arranged on a positive electrode 2. The average grain diameter of silicon crystal grains in the first layer and the second layer is 10 &mu m or larger. P-type dopant density in the first layer is 1× 10<18> per cm<3> to solution limit density at atmospheric pressure and the heat treatment temperature at the time of forming the first layer. The p-type dopant density in the second layer is reduced monotonously from the vicinity of a boundary in contact with the first layer to the vicinity of a p-n junction surface in contact with an n-type polycrystalline silicon layer 4, is the solution limit density at the atmospheric pressure and the heat treatment temperature, at forming of the first layer near the boundary and is 1× 10<15> -5× 10<17> per cm<3> near the p-n junction surface.

〈54〉 【Name of the patent】 **Thin film multi crystalline silicon solar cell and fabrication methods**

〈57〉 【Summary】

【Objective】 This patent offers a thin film multi crystalline silicon solar cell with excellent light-electricity conversion property, also provides feasible manufacturing methods which can achieve high efficiency for this cell.

【Scheme】 thin film multi crystalline silicon solar cell **10** consists of p-type multi crystalline silicon layer **3** which is on the top of positive electrode **2** and divided into first layer **32** and second layer **34**. The average silicon crystal size in the first layer and second layer is above 10 μm. P-type dopant concentration in the first layer is $1x10^{18}$atoms/cm$^3$ ~atmosphere pressure (?) which represents the solid solubility under the heat treatment temperature during first layer growth. P-type dopant concentration in the second layer decreases linearly from its interface with first layer towards the interface with n-type Si layer **4**, also near the interface the concentration is the solid solubility in heat treatment temperature during first layer growth, close to pn junction the concentration is $1x10^{15}$~$5x10^{17}$ atoms/cm$^3$.

【Scope】

【Claim 1】 The thin film multi crystalline silicon solar cell have following characteristics: substrate, positive electrode 2 formed on the substrate, p-type multi crystalline silicon formed on the electrode 2, n-type multi crystalline silicon formed on the p-type layer, and negative electrode formed on the n-type multi crystalline silicon. The p-type multi crystalline silicon divided into 2 layers, first layer is close to positive electrode while second layer sandwiched between the first layer and the n-type layer. The average grain size for the first and second layer is above 10 μm. P-type dopant concentration in the first layer is $1x10^{18}$atoms/cm$^3$ ~atmosphere pressure (?)which represents the solid solubility under the heat treatment temperature during first layer growth. P-type dopant concentration in the second layer decreases linearly from its interface with first layer towards the interface with n-type Si layer **4**, also near the interface the concentration is the solid solubility in heat treatment temperature during first layer growth, close to pn junction the concentration is $1x10^{15}$~$5x10^{17}$ atoms/cm$^3$.

【Claim 2】 The thin film multi crystalline silicon solar cell have following characteristics: substrate, p-type multi crystalline silicon formed on the substrate, n-type multi crystalline silicon formed on the p-type layer, positive electrode formed on the p-type layer which part without contact with n-type layer, and negative electrode formed on the n-type multi crystalline silicon. The p-type multi crystalline silicon divided into 2 layers, first layer is close to positive electrode while second layer sandwiched between the first layer and the n-type layer. The average grain size for the first and second layer is above 10 μm. P-type dopant concentration in the first layer is $1x10^{18}$atoms/cm$^3$ ~atmosphere pressure (?)which represents the solid solubility under the heat treatment temperature during first layer growth. P-type dopant concentration in the second layer decreases linearly from its interface with first layer towards the interface with n-type Si layer **4**, also near the interface the dopant concentration is the solid solubility in heat treatment temperature during first layer growth, close to pn junction the concentration is $1x10^{15}$~$5x10^{17}$ atoms/cm$^3$.

【Claim 3】 The thin film multi crystalline silicon solar cell have following characteristics: Positive electrode formed on the first layer without above mentioned second layer, others same as claim 2.

【Claim 4】 First layer processing: a metal layer formed on top of positive electrode, the metal should be able provide p-type dopant during crystallization with silicon. The average grain size above 10 mm generated while heating up this metal and amorphous silicon. P-type dopant concentration in the first layer is $1x10^{18}$atoms/cm$^3$ ~atmosphere pressure (?) which represents the solid solubility under the heat treatment temperature during first layer growth.
Third layer processing: Third layer consists of amorphous silicon, microcrystalline silicon or the mixture of both formed on top of the first layer.
Second layer processing: During heat or lamp treatment third layer crystallised and the grain size is above 10 μm. At same time, dopant atoms in the first layer diffused towards the third layer, so the second layer with p-type dopant formed.
Second layer and n-type layer on top of it formed pn junction.
Second layer resulted from above mentioned process had a dopant profile which linearly decreasing from first layer toward n-type layer. the dopant concentration near the interface is the solid solubility in heat treatment temperature during first layer growth, close to pn junction the concentration is $1x10^{15}$~$5x10^{17}$ atoms/cm$^3$.

【Claim 5】 First layer processing: a metal layer formed on top of positive electrode, the metal should be able provide p-type dopant during crystallization with silicon. The average grain size above 10 mm generated while heating up this metal and amorphous silicon. P-type dopant concentration in the first layer is $1x10^{18}$atoms/cm$^3$ ~atmosphere pressure (?) which represents the solid solubility under the heat treatment temperature during first layer growth.
Third layer processing: Third layer consists of amorphous silicon, microcrystalline silicon or the mixture of both formed on top of the first layer.
N-type layer processing: Amorphous silicon, microcrystalline silicon or the mixture of both deposits on top of third layer, forms n-type silicon layer.
Second layer processing: During heat or lamp treatment third layer crystallised and the grain size is above 10 μm. At same time, dopant atoms in the first layer diffused towards the third layer, so the second layer with p-type dopant formed.
Second layer and n-type layer on top of it formed pn junction.
Second layer resulted from above mentioned process had a dopant profile which linearly decreasing from first layer toward n-type layer. the dopant concentration near the interface is the solid solubility in heat treatment temperature during first layer growth, close to pn junction the concentration is $1x10^{15}$~$5x10^{17}$ atoms/cm$^3$.

【Claim 6】 First layer processing: a metal layer formed on top of positive electrode, the metal should be able provide p-type dopant during crystallization with silicon. The average grain size above 10 mm generated while heating up this metal and amorphous silicon. P-type dopant concentration in the first layer is $1x10^{18}$atoms/cm$^3$ ~atmosphere pressure (?) which represents the solid solubility under the heat treatment temperature during first layer growth.
Third layer processing: Third layer consists of amorphous silicon, microcrystalline silicon or the mixture of both formed on top of the first layer.

Second layer processing: During heat or lamp treatment third layer crystallised and the grain size is above 10 μm. At same time, dopant atoms in the first layer diffused towards the third layer, so the second layer with p-type dopant formed.
Second layer and n-type layer on top of it formed pn junction
Expose part of the first layer.
Positive electrode formed on top of exposed part of the first layer, negative electrode formed on n-type layer.
Second layer resulted from above mentioned process had a dopant profile which linearly decreasing from first layer toward n-type layer. the dopant concentration near the interface is the solid solubility in heat treatment temperature during first layer growth, close to pn junction the concentration is $1x10^{15}$~$5x10^{17}$ atoms/$cm^3$.

【Claim 7】 First layer processing: a metal layer formed on top of positive electrode, the metal should be able provide p-type dopant during crystallization with silicon. The average grain size above 10 mm generated while heating up this metal and amorphous silicon. P-type dopant concentration in the first layer is $1x10^{18}$atoms/$cm^3$ ~atmosphere pressure (?) which represents the solid solubility under the heat treatment temperature during first layer growth.
Third layer processing: Third layer consists of amorphous silicon, microcrystalline silicon or the mixture of both formed on top of the first layer.
N-type layer processing: Amorphous silicon, microcrystalline silicon or the mixture of both deposits on top of third layer, forms n-type silicon layer.
Second layer processing: During heat or lamp treatment third layer crystallised and the grain size is above 10 μm. At same time, dopant atoms in the first layer diffused towards the third layer, so the second layer with p-type dopant formed.
Expose part of the first layer.
Positive electrode formed on top of exposed part of the first layer, negative electrode formed on n-type layer.
Second layer resulted from above mentioned process had a dopant profile which linearly decreasing from first layer toward n-type layer. the dopant concentration near the interface is the solid solubility in heat treatment temperature during first layer growth, close to pn junction the concentration is $1x10^{15}$~$5x10^{17}$ atoms/$cm^3$.

Thin film multi crystalline silicon solar cell fabrication method (solar cell 10):

[0093] **Substrate**: stainless steel, **positive electrode 2**: silver and Al doped lead oxide double layer. Vacuum evaporate **Al layer 60(thickness: 500 nm)**, open chamber, so metal layer 60 exposed in air for 2 hours, DI water clean. Vacuum again; grow an **amorphous silicon layer 70 (thickness: 500 nm)**. Heat treatment: use temperature 50 °C below Si and Al phase temperature, that is 525 °C, for 1 hour, in the $N_2$ with 10% $H_2$ gas environment. In this heat treatment, Si atoms from amorphous Si layer 70 diffuse towards metal layer 60 and congregate to form a multi crystalline Si layer 32 between metal layer 60 and electrode 2 (thickness: 500nm, average Si grain size: 200 μm, p-type dopant Al atomic concentration: $1x\ 10^{19}/cm^3$).

【0040】

【Practical form of patent】 Following is detailed explanation for thin film multi-crystalline silicon solar cell and its fabrication methods.

【First implementation plan】 Figure 1 is cross section of thin film multi-crystalline silicon solar cell by this patent's first implementation plan. Figure 2(a)~(c), figure 3(a)~(d) and figure 4(a)~(d) show different processing methods of thin film multi-crystalline silicon solar cell as figure 1 presented.

【0041】 As fig. 1 shown, thin film multi-crystalline silicon solar cell 10 of first implementation plan comprise mainly of substrate 1, positive electrode (lower electrode) 2, p-type multi-crystalline silicon layer 3, n-type multi-crystalline silicon layer 4 and negative electrode (upper electrode) 5.

【0042】 Substrate 1: There is no restriction for the material used in this substrate, as long as it can support the multi layers and endure process heating. For example, it can be silicon substrate such as single crystalline silicon or multi crystalline silicon; it can be stainless steel substrate and high temperature glass, etc.

【0043】 To prevent positive electrode peeling off from substrate, a lead oxide stress buffer film (not show in the figures) can be put on the substrate, also can be added are some barrier layers (not show in the figures) that preventing impurity diffusion from substrate 1 to positive electrode 2, and from electrode 2 to p-type multi crystalline silicon layer 3. ...

【0044】 Positive electrode 2: It can be silver, aluminum or titanium; also can be multi layer metal film consisting of one or more above mentioned metals, or transparent glass electrode. At the interface of electrode 2 and silicon layer 3, it is better to make a buffer film to prevent p-type silicon peeling off from the electrode (not shown in figure). Also a barrier film can be added between 2 and 3 to prevent impurity diffusion. And tin oxide or tin oxide with indium added can be used to form electrode 2.

【0045】 P-type silicon layer 3 divided into 2 layers, layer 32 is close to electrode 2 sides and layer 34 is close to n-type silicon side. As above mentioned, layers 32 and 34 have silicon grain size of above 10 μm.

【0046】 First layer 32 contains p-type dopant $1x10^{18}/cm^3$~atmosphere pressure which is in the range of solid solubility under first layer heat treatment temperature. Therefore this p-type dopant has to be an element that could form crystalline structure with silicon. For example, p-type dopant Al's concentration can exceed $1x10^{18}/cm^3$.

【0047】 In second layer 34 the p dopant concentration became a slope distribution, that is, at interface with first layer, its concentration is limited by solid solubility, and near pn junction its concentration is at range of $1x10^{15}/cm^3$~$5x10^{17}/cm^3$. In either of second layer 34 or first layer 32 the p-type dopant is same.

【0048】 In n-type silicon layer 4 contains n dopant. The dopant concentration is in the range of $5x10^{18}/cm^3$~$1x10^{20}/cm^3$, better in $1x10^{19}/cm^3$~$5x10^{19}/cm^3$. Simulation indicates that maximum efficiency can be achieved by this dopant concentration. N-type dopant can be phosphorus, arsenic, or antimony such V-group elements.

【0049】 To ensure good conductivity and obtain longer lifetime, the average grain size in n-type mc silicon 4 should be lager than 10 μm. The pn junction formed at interface of the second layer 34 and n-type layer 4.

【0050】 Negative electrode 5 formed on top of n-type layer4, it can be made of Al, Ag, and Ti, etc, metal material. The shape of the electrode is grid for higher efficiency. Also it can use transparent glass as electrode. And, anti-reflection layer (not shown in figures) can be added on top of electrode 4 to increase the efficiency.

【0051】 Refering to fig. 2(a)~(c), fig. 3(a)~(d), and fig.4 (a)~(d), following is explanation of two example of manufacturing methods of solar cell 10(fig. 1).

【0052】 First method: as mentioned above, firstly, a metal layer 60 (which can crystallize with silicon and supply p-type dopant) formed on top of electrode 2. Then an amorphous silicon layer 70 formed on top of metal layer 60, heat treatment this two layers generated first layer 32, which sits on top electrode 2 and substrate. Third layer 80 formed on top of first layer 32 and second layer 34 formed by thermal or light annealing. N-type layer formed on top of second layer 34 and so the pn junction built up.

【0053】 There is no restriction on how to form first layer 32, although it can follow the procedure shown on fig. 2(a)~(c). Fig. 2(a) shows that firstly positive electrode (lower electrode) formed on top of substrate; then metal layer 60 deposited on top of pos. electrode. Then amorphous silicon layer 70 formed.

【0054】 Metal layer 60 should be able co-crystallize with silicon and supply p-type dopant into silicon. It can be made of boron, aluminum, gallium, or indium, among those Al is best choice. In this patent instruction book, even the element formed metal layer is non-metal, it still called "metal layer 60". The method used for this layer can be vacuum physical evaporating and sputtering, or gas phase growth, etc. From controlling fab cost point of view, physical evaporating is best choice. Metal layer 60's thickness can be from 500 nm ~1 μm, best range is 300 nm ~500 nm.

【0055】 The method for deposit amorphous silicon layer 70 can be physical evaporating and sputtering or gas phase growth. From controlling fab cost point of view, physical evaporating is best choice. Before the deposition of amorphous silicon layer 70, metal layer 60 should exposed in atmosphere with oxygen. Organic solvent such as acetone and alcohol, and DI water can be used for cleaning the surface before silicon layer deposition. This can ensure that the average silicon grain size in first layer 32 keep above 10 μm after thermal annealing. The thickness of amorphous silicon layer 70 is 500

nm ~ 1 μm, better control at 300 nm ~ 500 nm. Silicon layer 70 and metal layer 60 should have roughly same thickness.

【0056】 Thermal annealing temperature for metal layer 60 and amorphous silicon layer 70 should 20~100 °C below their recrystallizition temperature, best choice is 50 °C below the temperature. Fig. 2(b) shows that silicon atoms in layer 70 diffused into metal layer 60 during thermal process, formed first layer 32 with p-type dopant concentration of $1x10^{18}/cm^3$~atmosphere pressure and average grain size above 10 □m. At this time, residue metal layer 62 was left on top of layer 32.

【0057】 Thermal process was conducted at above mentioned temperature, in $N_2$, Ar inert gas or $H_2$ and inert gas mixture environment for 30 min ~ 24 hrs. For instance, in case of metal layer 60 is Al, thermal annealing temperature should be at 400 to 570 °C, best choice would be 500 ~ 550 °C. Thermal process time should be 30 min ~ 5 hrs. Thermal process time should be 1~2 hrs when the temperature at 500 ~550 °C. Or, the temperature should be 50 °C below recrystallization temperature.

【0058】 Fig. 2(c) shows that residue metal layer 62 was removed, layer 32 exposed on the surface. Remove layer 62 can be done with etching. For example, in case of Al is layer 62, phosphorus acid chemical etching and chlorine gas reactive ion etching can be used.

【0059】 Fig. 3(a) shows that process of the third layer. Layer 80 is amorphous or microcrystalline silicon or the mixture of both deposited on top of layer 32. If the layer formed by microcrystalline silicon the average grain size should be less than 10 nm. Layer 80's processing can be vacuum evaporating, sputtering, or ion-plating[? Is there such thing exists? - Aihua]. Plasma gas phase growth is also suitable. Physical depositing is best choice for cost consideration. To decide the thickness of third layer 80 should consider second layer 34, which is part of layer 80, and n-type mc silicon layer 4. It can be at a range of 1~50 μm, better at 1.5~10 μm.

【0060】 Fig. 3(b) shows the second layer processing shown. This layer 34 formed by thermal or light annealing to diffuse p-type dopant into it. Under heat or laser the first layer 32 as a seed crystal make layer 80 crystallized, the average grain size is above 10 μm. At same time, parts of p-type dopant in layer 32 diffuse into third layer 80 and the distribution of dopant in layer 34 is slope shape.

【0061】 Generally, when dopant diffuse from source layer (layer 32) to another layer (layer 80), the concentration will getting lower with longer the distance, this is the reason for above mentioned dopant slope distribution. And the slope is getting steeper when the time is shorter. So the diffusion temperature or time should adjusted to accommodate third layer 80's thickness and also keep p-type dopant concentration at n-type layer interface at $1x10^{15}/cm^3$~$5x10^{17}/cm^3$. Because of p-type dopant diffuse from layer 32 into layer 80 to form layer 34, layer 32 will get thinner when layer 34 formed.

Therefore, as Fig. 3(a) shows, the interface F38 between first layer 32 and third layer 80, with p dopant diffusing into layer 80, F38 slowly moves towards substrate. Fig. 3(b) shows that interface F3 formed between layer 32 and layer 34 after layer 34 appearances.

【0062】 Thermal or light can be used for crystallize the third layer 80. Rapid annealing methods such as thermal annealing, lamp annealing or laser annealing is suitable.

【0063】 To form pn junction is forming an n-type layer on top of second layer. Fig. 3(c) shows that n-type silicon layer 4 formed by adding n-type dopant to the layer above layer 34. The interface of pn junction is F10. The doping methods can be commonly used diffusion or ion-implantation. There is no restriction for thickness of n-type layer 4, normal thin film solar cell's n layer thickness should be sufficient.

【0064】 Fig. 3(d) shows that negative electrode formed on top of n layer 4. So far the basic structure of thin film mc silicon solar cell 10 is finished. Negative electrode 5 can be achieved by vacuum evaporating of Al or other metal grid pattern.

【0065】 From Fig. 4(a) ~(d), Second fabrication method was explained for solar cell 10.

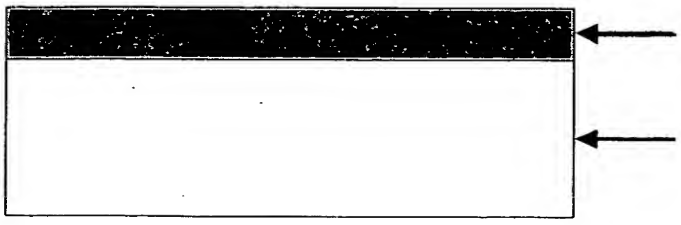

Fig. 1

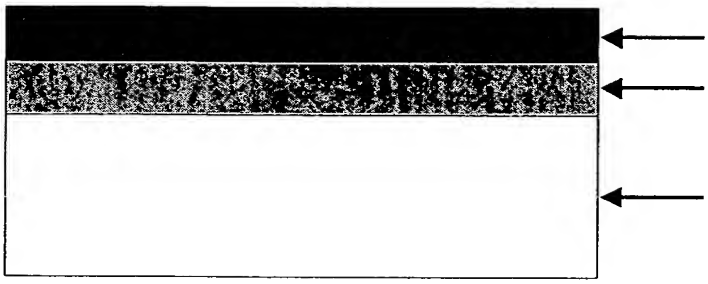

Fig. 2

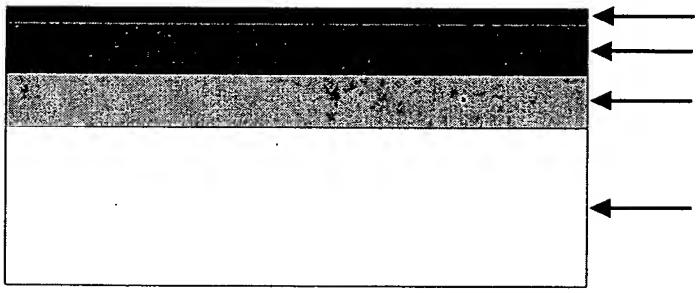

Fig. 3

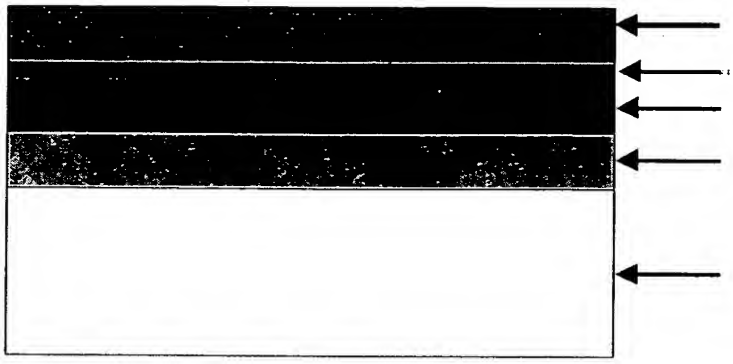

Fig. 4

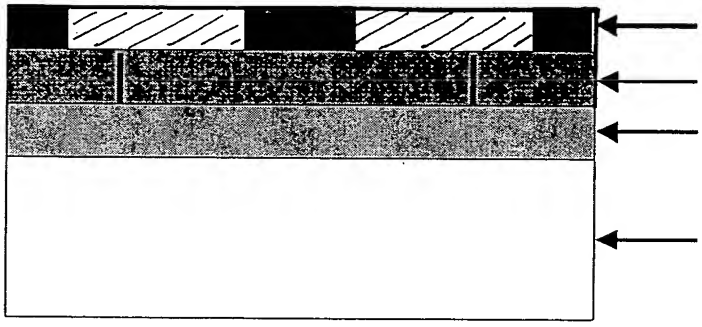

Fig 5

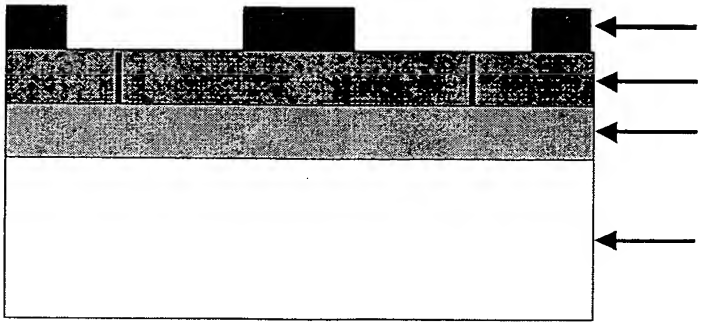

Fig 6

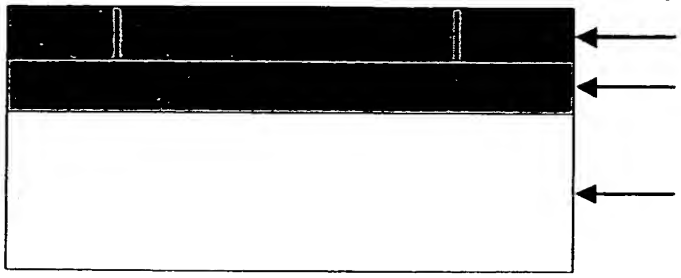

Fig 7

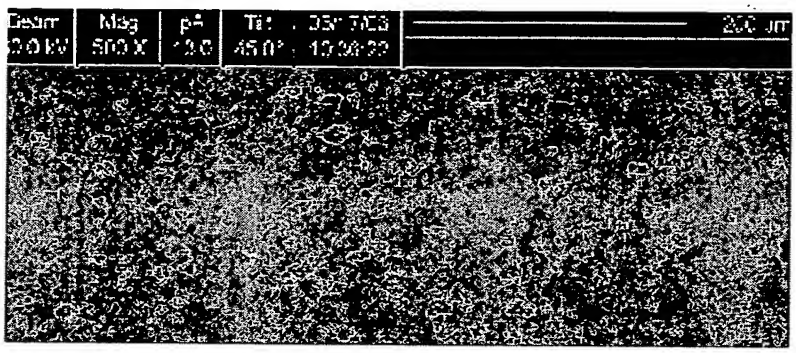

Fig 8

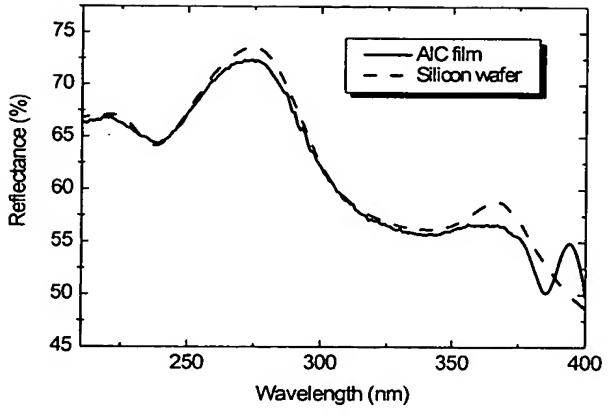


Fig. 9

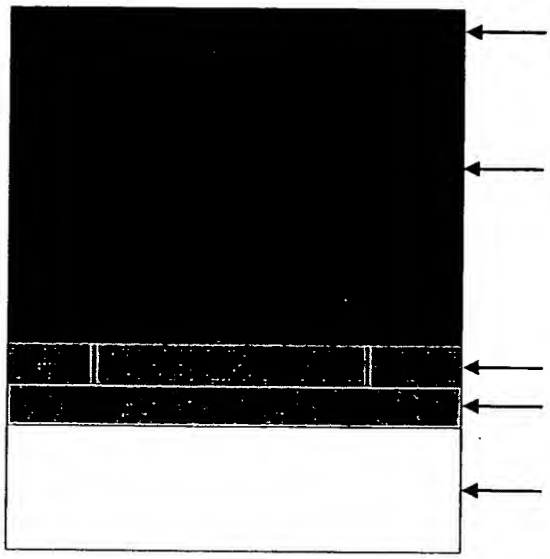

Fig.10

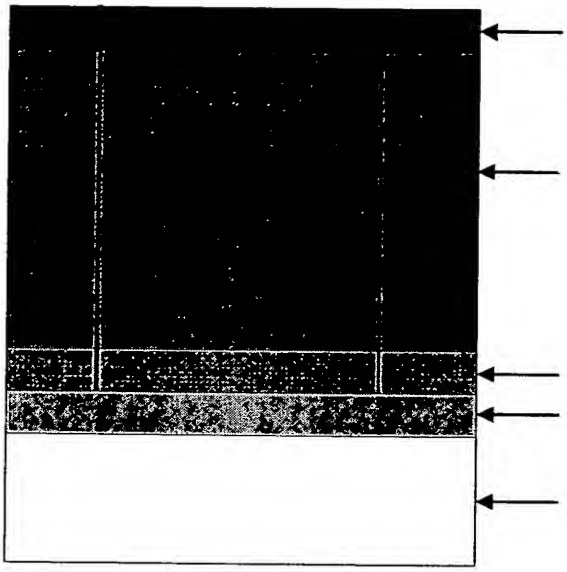

Fig. 11

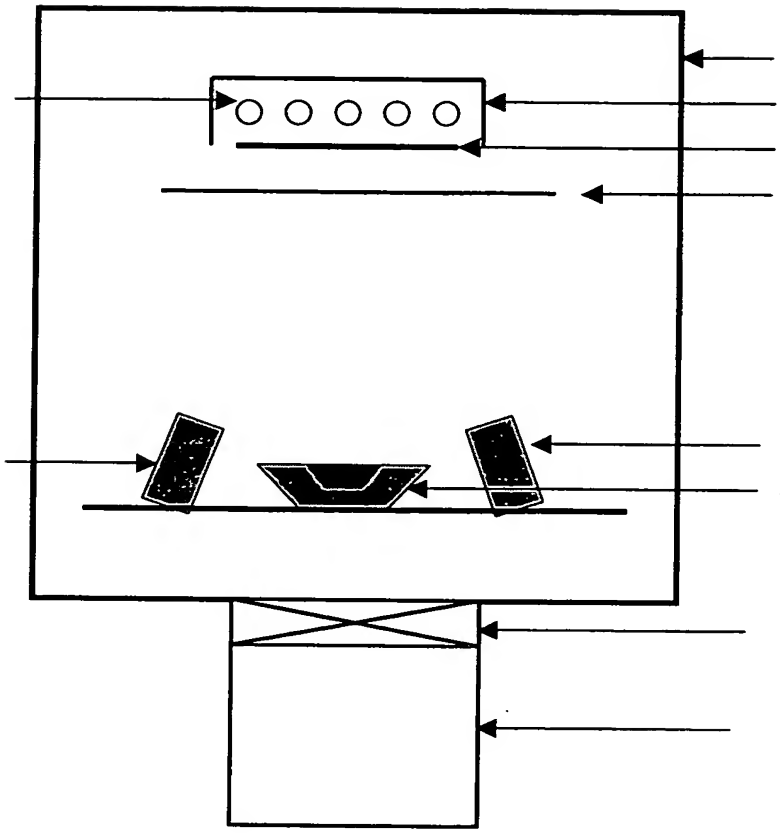

**Fig. 12**